501.38505CX1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: N. YAMAMOTO, et al.

Serial No.: To be assigned

Filed: January 21, 2004

For: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND METHOD FOR MANUFACTURING THE SAME

Group: 2825 (previous)

Examiner: C.A. LUU (previous)

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97 & 1.98

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450 January 21, 2004

Sir:

In the matter of the above-identified application, it is requested that the Examiner consider the documents listed on the attached form equivalent to Form PTO-1449. Copies of the documents are not being submitted herewith because they are of record in parent application Serial No. 09/577,671, filed May 25, 2000.

This information disclosure statement is being submitted within three months of the filing date.

It is respectfully requested that this information disclosure statement be considered by the Examiner.

Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit account of

Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (Case: 501.38505CX1), and please credit any excess fees to such deposit account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

Ronald J. Shore
Registration No. 28,577

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Attachments

Form PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DKT. NO.	SERIAL NO.
		501.38505CX1	To be assigned
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)		APPLICANT: YAMAMOTO et al.	
		FILING DATE: January 21, 2004	GROUP:

U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date
		2001/0042344A1	11/22/01	Ohmi et al.			02/15/01
		6,323,115B1	11/27/01	Tanabe et al.			05/20/99
		2002/0004263A1	01/10/02	Tanabe et al.			08/15/01
		4,505,028	05/19/85	Kobayashi, et al.			
		6,362,086	03/26/02	Weimer et al.			

FOREIGN PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Country	Class	Subclass	Translation /Abstract	
							Yes	No
		11-330468	11/99	Japan				
		10-233505	09/98	Japan			XX	
		9-298170	11/97	Japan			XX	
		59-132136	07/84	Japan				XX
		7-94716	04/95	Japan			XX	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

		Advanced Metallization Conference Japan Session, Tokyo Univ. 1995, Polymetal Gate Process-Ultrathin WSiN Barrier Layer Impermeable to Oxidant Indiffusion during Si Selective Oxidation

Examiner	Date Considered

Form PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DKT. NO.	SERIAL NO.
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		FILING DATE: January 21, 2004	GROUP

U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date
		2001 0051406 A1	12/13/01	Weimer et al.			
		6,239,044	05/29/01	Kashiwagi et al.			
		6,214,683	04/10/01	Xiang et al.			
		6,228,752 B1	05/01	Miyano			
		6,162,741	12/00	Akasaka, et al.			
		6,306,698 B1	10/01	Wieczovek et al.			
		6,287,903 B1	09/01	Okuno, et al.			

FOREIGN PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Country	Class	Subclass	Translation /Abstract	
							Yes	No
		60-160667	1985	Japan				

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner	Date Considered